REMARKS

The foregoing amendments and the following remarks are responsive to the February 10, 2005 Office Action. Claims 1, 6, 8, and 12 are currently amended, Claims 2-5 and 9 remain as originally filed, and Claims 7, 10-11, and 13-18 remain as previously presented, and Claim 19 is new. Thus, Claims 1-19 are presented for further consideration. Please enter the amendments and reconsider the claims in view of the following remarks.

Response to Provisional Rejection of Claims 1 and 10-14 for Obviousness-Type Double Patenting

In the February 10, 2005 Office Action, the Examiner provisionally rejects Claims 1 and 10-14 under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over Claims 1, 3, 9-11, 13, 19, and 20 of copending U.S. Patent Application No. 10/765,488.

While Applicants traverse this provisional rejection, Applicants are submitting herewith a Terminal Disclaimer to overcome the obviousness-type double patenting rejection in order to expedite allowance of Claims 1 and 10-14 of the present application. Applicants respectfully request that the Examiner withdraw the provisional rejection and pass Claims 1 and 10-14 to allowance.

Response to Rejection of Claims 1 and 12-14 Under 35 U.S.C. § 103(a)

In the February 10, 2005 Office Action, the Examiner rejects Claims 1 and 12-14 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2003/0075789 A1 to Kawamura et al. ("Kawamura"). The Examiner states that Kawamura discloses all the limitations of Claims 1 and 12-14, except for "the first register addressing the identical integrated circuits ... on a first lateral portion ... and the second register addressing the identical integrated circuits on a second lateral portion." However, the Examiner states that it would have been obvious to one of ordinary skill in the art to provide this limitation since rearranging parts of an invention or discovering the optimum or workable ranges involves only routine skill in the art.

Claim 1

Applicants have amended Claim 1 to recite (emphasis added):

1. A memory module comprising:
a printed circuit board having a first lateral portion and a second lateral portion;
a plurality of identical integrated circuits mounted in at least two rows onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits; and

a first register and a second register connected to the control logic bus, **the first register addressing the identical integrated circuits located on the first lateral portion and not addressing the identical integrated circuits located on the second lateral portion, and the second register addressing the identical integrated circuits located on the second lateral portion and not addressing the identical integrated circuits located on the first lateral portion.**

Applicants submit that the claimed invention of amended Claim 1 is non-obvious over Kawamura. Figures 6 and 7 of Kawamura illustrate a memory module utilizing stacked memory integrated circuits (ICs) with two registers on a first side of the printed circuit board (PCB) and a third register on a second side of the PCB. Kawamura does not disclose or suggest how the registers are coupled to the memory ICs or that the first register addresses only the ICs on the first lateral portion of the PCB and the second register addresses only the ICs on the second lateral portion of the PCB. Therefore, Kawamura does not teach or disclose the claimed invention recited by Claim 1.

The Examiner states that the claimed invention of Claim 1 is merely a rearrangement of the parts disclosed by Kawamura, and that such a rearrangement involves only routine skill in the art, so that Claim 1 is obvious over Kawamura. The Examiner further states that the claimed invention of Claim 1 is merely an optimum or workable range of general conditions which are disclosed in the prior art, the discovery of which involves only routine skill in the art.

However, Applicants respectfully point out that Kawamura discloses nothing regarding the electrical connections between the register ICs and the memory ICs. Therefore, the claimed invention of Claim 1 can not be considered to be a mere rearrangement of the elements disclosed by Kawamura. Furthermore, because Kawamura discloses nothing regarding the electrical connections between the register ICs and the memory ICs, the claimed invention of Claim 1 can not be considered to be a mere optimization of ranges disclosed by Kawamura.

Kawamura presumably conforms to the Joint Electron Device Engineering Council (JEDEC) standards for addressing registers which do not disclose the claimed invention of Claim 1. For example, in the JEDEC Standard No. 21-C, 420.2 – 168 Pin, PC133 SDRAM Registered DIMM Design Specification, Revision 1.4, Release 11s, February 2002, which is of record in the present application, each of the register ICs addresses each of the memory ICs. See, e.g., Block Diagrams for Raw Card Versions A-G on pages 9-15 and Net Structure Routing for Address and Control on pages 57-60. In contrast, the claimed invention of Claim 1 has "a first

register addressing the identical integrated circuits located on the first lateral portion and not addressing the identical integrated circuits located on the second lateral portion" and has "a second register addressing the identical integrated circuits located on the second lateral portion and not addressing the identical integrated circuits located on the first lateral portion." Thus, the cited JEDEC standards for addressing registers do not disclose or suggest the claimed invention of Claim 1.

Furthermore, the claimed invention of Claim 1 is not a mere rearrangement or optimum range of the elements disclosed by the prior art. The Examiner cites In re Japikse, 181 F.2d 1019, 86 U.S.P.Q. 70 (C.C.P.A. 1950) in rejecting Claim 1 as being a mere rearrangement of parts which involves only routine skill in the art. However, in Japikse, the position of a starting switch for a hydraulic power press was held to have no effect on the operation of the device, so the position of the starting switch was held to not be a patentable feature over the prior art. In contrast, the coupling of the first and second registers to the ICs of the first and second lateral portions, respectively, as recited by Claim 1, has an advantageous effect on the operation of the memory module. As described by the present specification at paragraph [0035], the claimed configuration recited by Claim 1 "allows closer matching of timing performance for the signals from the integrated circuits 102, improves the timing performance, and provides greater performance timing margins than traditional design guidelines in which each integrated circuit in a row of integrated circuits 102 is connected to a single register." Thus, the claimed invention recited by Claim 1 is not a mere rearrangement, but provides improved operation of the memory module.

In addition, the claimed invention of Claim 1 is not a mere optimization of ranges disclosed by the prior art. The Examiner cites In re Aller, 220 F.2d 454, 456, 105 U.S.P.Q. 233, 235 (C.C.P.A. 1955) in rejecting Claim 1 to note that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. However, in Aller, a claimed process was found to be obvious in view of a prior art process which utilized different temperatures and concentrations but still disclosed the general conditions of the claim. In contrast, the coupling of the first and second registers to the ICs of the first and second lateral portions, respectively, as recited by Claim 1, is not a mere change of parameters as compared to the prior art. By disclosing that each of the register ICs addresses each of the memory ICs, the prior art fails to disclose the general conditions of the claimed

invention recited by Claim 1. Thus, the claimed invention recited by Claim 1 is not a mere optimization of ranges disclosed by the prior art.

For the foregoing reasons, Applicants submit that the claimed invention recited by Claim 1 is non-obvious over Kawamura. Applicants respectfully request that the Examiner withdraw the rejection of Claim 1 and pass Claim 1 to allowance.

Claim 12

Applicants have amended Claim 12 to recite (emphasis added):

> 12. A memory module comprising:
> a printed circuit board;
> a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;
> a control logic bus connected to the plurality of identical integrated circuits; and
> a first register and a second register connected to the control logic bus, **the first register addressing only the identical integrated circuits located in the first row and the second row of identical integrated circuits on a first lateral portion of the at least one surface of the printed circuit board, and the second register addressing only the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral portion of the at least one surface of the printed circuit board**.

For the reasons discussed above in relation to amended Claim 1, Applicants submit that the claimed invention of amended Claim 12 is non-obvious over Kawamura. Applicants respectfully request that the Examiner withdraw the rejection of Claim 12 and pass Claim 12 to allowance.

Claims 13 and 14

Each of Claims 13 and 14 depends from Claim 12, so each of Claims 13 and 14 includes all the limitations of Claim 12, as well as other limitations of particular utility. For the reasons discussed above, Applicants submit that Claims 13 and 14 are non-obvious over Kawamura. Applicants respectfully request that the Examiner withdraw the rejection of Claims 13 and 14 and to pass these claims to allowance.

Response to Rejection of Claims 6-9 and 15-18 Under 35 U.S.C. § 103(a)

In the February 10, 2005 Office Action, the Examiner rejects Claims 6-9 and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of U.S. Patent No. 6,594,167 B1 issued to Yamasaki et al. ("Yamasaki").

Claims 6-9

Applicants submit that Yamasaki does not disclose or suggest the limitations of Claim 1 which are not taught or suggested by Kawamura. Therefore, Applicants submit that Claim 1 is non-obvious over Kawamura in view of Yamasaki.

As described herein, Applicants have amended Claims 6 and 8. Each of Claims 6 and 8 depends from Claim 1, Claim 7 depends from Claim 6, and Claim 9 depends from Claim 8. Therefore, each of Claims 6-9 includes all the limitations of Claim 1, as well as other limitations of particular utility. Applicants submit that Claims 6-9 are non-obvious over Kawamura in view of Yamasaki. Applicants respectfully request that the Examiner withdraw the rejection of Claims 6-9 and to pass these claims to allowance.

Claims 15-18

Applicants submit that Yamasaki does not disclose or suggest the limitations of Claim 12 which are not taught or suggested by Kawamura. Therefore, Applicants submit that Claim 12 is non-obvious over Kawamura in view of Yamasaki.

Each of Claims 15 and 17 depends from Claim 12, Claim 16 depends from Claim 15, and Claim 18 depends from Claim 17. Therefore, each of Claims 15-18 includes all the limitations of Claim 12, as well as other limitations of particular utility. Applicants submit that Claims 15-18 are non-obvious over Kawamura in view of Yamasaki. Applicants respectfully request that the Examiner withdraw the rejection of Claims 15-18 and to pass these claims to allowance.

Response to Rejection of Claims 2-5 Under 35 U.S.C. § 103(a)

In the February 10, 2005 Office Action, the Examiner rejects Claims 2-5 under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of U.S. Patent No. 6,705,877 B1 issued to Li et al. ("Li").

Applicants submit that Li does not disclose or suggest the limitations of Claim 1 which are not taught or suggested by Kawamura. Therefore, Applicants submit that Claim 1 is non-obvious over Kawamura in view of Li.

Each of Claims 2-5 depends from Claim 1, so each of Claims 2-5 includes all the limitations of Claim 1, as well as other limitations of particular utility. Applicants submit that Claims 2-5 are non-obvious over Kawamura in view of Li. Applicants respectfully request that the Examiner withdraw the rejection of Claims 2-5 and to pass these claims to allowance.

Comments on New Claim 19

Applicants have added new Claim 19 which recites:

19. A memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted on the printed circuit board in a first row and a second row;

a control logic bus connected to the plurality of identical integrated circuits; and

a first register connected to the control logic bus, the first register addressing the identical integrated circuits located in the first row and the second row on the first lateral portion and not addressing the identical integrated circuits located in the first row and the second row on the second lateral portion; and

a second register connected to the control logic bus, the second register addressing the identical integrated circuits located in the first row and the second row on the second lateral portion and not addressing the identical integrated circuits located in the first row and the second row on the first lateral portion.

For the reasons discussed above in relation to amended Claim 1, Applicants submit that the claimed invention of Claim 19 is patentable. Applicants respectfully request that the Examiner consider the patentability of new Claim 19 and to pass Claim 19 to allowance.

Summary

For the foregoing reasons, Applicants submit that Claims 1-19 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 4/27/05 By: _____

Bruce S. Itchkawitz
Registration No. 47,677
KNOBBE, MARTENS, OLSON & BEAR, LLP
Attorney of Record
2040 Main Street
Fourteenth Floor
Irvine, CA 92614
(949) 760-0404

1678835
042205